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Reply to Office Action of October 20, 2004

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the above-identified application:

Claim 1 (currently amended): A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

developing at least one simulation test vector using a PLD design automation software tool, each simulation test vector used to test a simulated model of the programmed PLD;

testing a simulated model of the programmed PLD using each of the simulation test vectors;

translating at least one simulation test vector into at least one device level test vector that is while testing the simulation test model, each device level test vector being in a format readable by the PLD test device; and

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results.

Claim 2 (original): The method of Claim 1, wherein all of the simulated test vectors are translated into a corresponding device level test vector.

Claim 3 (currently amended): The method of Claim 1, further comprising:

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtaining simulation test results while testing the simulation test model; and

comparing the simulation test results with the device level test results.

Claim 4 (original): The method of Claim 1, further comprising:

developing a software model of the programmed PLD using the design automation software tool; and

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translating the software model of the programmed PLD into the simulated model
of the programmed PLD using a simulation software tool.

Claim 5 (currently amended): The method of Claim 4, wherein the simulation software
tool translates the simulation test vectors into the device level test vectors while testing
the simulation test model.

Claim 6 (original): The method of Claim 5, wherein each of the device level test vectors
include stimulus data and expected results data.

Claim 7 (original): The method of Claim 1, further comprising:

    generating at least one data file; and

    storing each of the device level test vectors in the data files.

Claim 8 (original): The method of Claim 7, further comprising:

    compressing the data files;

    storing the compressed data files on a memory storage device; and

    decompressing the compressed data files to recover the device level test vectors.

Claim 9 (original): The method of Claim 1, further comprising:

    developing a software model of the programmed PLD using a design automation
software tool; and

    synthesizing the software model of the programmed PLD using a design synthesis
software tool.

Claim 10 (original): The method of Claim 9, further comprising:

    generating a PLD program file from the synthesized software model.

Claim 11 (original): The method of Claim 10, further comprising:

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downloading the PLD program file into an integrated PLD circuit to create the programmed PLD.

Claim 12 (original): The method of Claim 1, further comprising:

developing a software model of the programmed PLD using a design automation software tool;

synthesizing the software model of the programmed PLD using a design synthesis software tool;

translating the synthesized software model into a post-synthesis simulated model of the programmed PLD using the simulation software; and

testing the post-synthesis simulated model of the programmed PLD using each of the simulation test vectors to obtain post-synthesis simulation test results.

Claim 13 (currently amended): A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

developing at least one simulation test vector using a PLD design automation software tool, each simulation test vector used to test a simulated model of the programmed PLD;

testing a simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results:

translating at least one simulation test vector into at least one device level test vector that is while testing the simulation test model, each device level test vector being in a format readable by the PLD test device;

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results; and

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and

comparing the simulation test results with the device level test results.

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Claim 14 (original): The method of Claim 13, wherein all of the simulated test vectors are translated into a corresponding device level test vector.

Claim 15 (original): The method of Claim 13, further comprising:

developing a software model of the programmed PLD using the design automation software tool; and

translating the software model of the programmed PLD into the simulated model of the programmed PLD using a simulation software tool.

Claim 16 (currently amended): The method of Claim 15, wherein the simulation software tool translates the simulation test vectors into the device level test vectors while testing the simulation test model.

Claim 17 (original): The method of Claim 16, wherein each of the device level test vectors include stimulus data and expected results data.

Claim 18 (original): The method of Claim 13, further comprising:

generating at least one data file; and

storing each of the device level test vectors in the data files.

Claim 19 (original): The method of Claim 18, further comprising:

compressing the data files;

storing the compressed data files on a memory storage device; and

decompressing the compressed data files to recover the device level test vectors.

Claim 20 (original): The method of Claim 13, further comprising:

developing a software model of the programmed PLD using a design automation software tool; and

synthesizing the software model of the programmed PLD using a design synthesis software tool.

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Claim 21 (original): The method of Claim 20, further comprising:

 generating a PLD program file from the synthesized software model.

Claim 22 (original): The method of Claim 21, further comprising:

 downloading the PLD program file into an integrated PLD circuit to create the programmed PLD.

Claim 23 (original): The method of Claim 13, further comprising:

 developing a software model of the programmed PLD using a design automation software tool;

 synthesizing the software model of the programmed PLD using a design synthesis software tool;

 translating the synthesized software model into a post-synthesis simulated model of the programmed PLD using the simulation software; and

 testing the post-synthesis simulated model of the programmed PLD using each of the simulation test vectors to obtain post-synthesis simulation test results.

Claim 24 (currently amended): A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

 developing a software model of the programmed PLD using a design automation software tool;

 translating the software model of the programmed PLD into a simulated model of the programmed PLD using a simulation software tool;

 developing at least one simulation test vector using PLD the design automation software tool, ~~each simulation test vector used to testing the simulated model of the programmed PLD~~;

 <u>testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results;</u>

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     translating at least one simulation test vector into at least one device level test vector ~~that is~~ while testing the simulation test model, each device level test vector being in a format readable by the PLD test device;

     testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results;

     ~~testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and~~

     comparing the simulation test results with the device level test results.

Claims 25-53 (canceled).

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